UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,533	12/20/2001	Fumio Arakawa	NIT-311	2166

7590 10/27/2004

Mattingly, Stanger & Malur, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
HOANG, PHUONG N	
ART UNIT	PAPER NUMBER
2126	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,533	ARAKAWA, FUMIO	
	Examiner	Art Unit	
	Phuong N. Hoang	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 11 are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

i. said threads, and said priorities – claim 1;

ii. said threads – claim 2;

iii. the processor hardware, and said threads – claim 3;

iv. said threads – claims 5 and 10;

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 - 3, 5 – 6, and 9 - 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diefendorff "Simultaneous Multithreading Exploits Instruction – and Thread-Level Parallelism" pages 1 – 8.

6. **As to claim 1,** Diefendorff teaches a processor comprising the steps of:

plurality of program counters (counters for threads, page 4 lines 19 – 25);

one or a plurality of instruction execution parts (execution units, page 1 lines 29 – 35 and page 2 lines 56 - 62); and

means for selectively supplying for a plurality of threads instruction flows (threads, instruction streams, onto the execution units, page 1 lines 29 – 35 and page 3 lines 15 – 25) to the one a plurality of instruction parts, each of the threads corresponding each of the program counters (a counter for each thread, page 4 lines 19 – 25),

wherein the threads can be executed either simultaneously (simultaneous multithread processors, page 2 lines 26 – 62) or in time multiplex (thread-level parallelism, page 2 lines 26 – 62),

wherein the priorities among the threads in parallel (The two threads were .... prioritizes fetch from threads, page 4 lines 11 – 19) and generates the same result (The real beauty of SMT is that as threads execute, ... A single thread ... alternatively ... low ILP, page 2 lines 56 – 62) as serial execution according to the priorities in parallel,

processor has changeable execution would generate (shift their attention from ILP to explicit thread-level parallelism, page 2 lines 26 – 30).

Diefendorff does not explicitly teaches the thread are executing in time multiplex. However, Diefenforff teaches threads are executing in parallel (thread-level parallelism, page 2 lines 26 – 30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that thread running in parallel would work the same as in time multiplex because multiple threads can run in the same time.

7. **As to claim 2**, Diefendorff teaches the step of whereby made possible to reduce hardware (hardware resources are sized for a single-thread and that additional SMT threads are treated as opportunistic, page 3 lines 49 – 55) volume data deliveries between the threads (threads running asynchronously, page 3 lines 45 - 56) through a shared resource (affectively shared) the processor and by causing the threads to share part or the whole of processor resources except the program counters (each counter for each thread, page 4 lines 19 – 25).

8. **As to claim 3**, Diefendorff teaches the step of wherein the number of repeats as a first criterion of priority (putting thread to sleep and waking it, page 6 lines 12 – 20) the is enabled to achieve synchronization (threads running asynchronously, page 3 lines 45 – 55) among processor hardware the threads without requiring any intervening instruction by using priorities among the threads as a second criterion of priority.

9. **As to claim 5**, Diefendorff teaches the steps of threads other than that having top priority can be executed without a conflict by confining data dependency among the threads so that data flow in only one direction and executing a data using thread only when it is the top priority thread (threads are asynchronous running, page 3 lines 45 – 55 and page 6 lines 5 – 10), they are not be conflicted and so the use of undefined data can be eliminated.

10. **As to claim 6**, Diefendorff teaches the step of wherein a storing location for data to be used in inter-thread (interthread, page 4 lines 11 – 15) data communication confined.

11. **As to claim 9**, Diefendorff teaches the step of wherein the data storing location is part of a memory (it is inherent that memory for storing data).

12. **As to claim 10**, Diefendorff teaches the step of having a thread priority raising instruction threads lower in priority to facilitate changing priority among the threads (prioritize threads, col. 4 lines 11 – 19).

13. **As to claim 11**, Diefendorff teaches the step of having a data definition synchronizing instruction (instructions, page 1 lines 52 - 62 and page 3 lines 45 – 62) for other threads make synchronization threads after synchronization.

14. Claims 4, and 7 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diefendorff "Simultaneous Multithreading Exploits Instruction – and Thread-Level Parallelism" pages 1 – 8 in view of Thayer, US patent no. US patent no. 6,154,831.

15. **As to claim 4**, Diefendorff does not explicitly teach the steps comprising of a buffer for temporarily holding the execution results of threads other than that having top priority.

Thayer teaches the step comprising of buffer (buffer, col. 11 lines 45 – 60) for temporarily holding the execution results of threads other than that having top priority thereby making possible conflict-free execution of such other threads by storing them in their primary storing location after the completion or synchronization report of processing with higher priority.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Diefendorff and Thayer's system because Thayer's buffer would keep the data in an area of the storage to be organized and so avoid the conflict execution of threads.

16. **As to claims 7 and 8**, Thayer teaches the step of wherein plurality of locations (the storage of locations are located, col. 14 lines 45 – 60) are defined for data storage,

independent of each and differentiated by the combination of threads and the direction of communication.

Conclusion

17. The prior art made of record but not relied upon request is considered to applicant's disclosure.

Flauthner et al, "Thread-level Parallelism and Interactive Performance of Destop Applicants", pages 1 – 10, demonstrating superscalar processor in a client-server environment.

Lo et al, "Converting Thread-Level Parallelism to Instruction-Level Parallelism via Simultaneous Multithreading" pages 322 – 354, domonstrating a alternative of running a multithreaded processor.

Park et al, US patent no. 5,881,307, demonstrating a superscalar processor including execution units.

White et al, US patent no. 5,574,928, demonstrating a superscalar microprocessor with a plurality of buses for transferring segments.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is

(571)272-3763. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ph
October 15, 2004

MENG-AI T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100